1. A resonant tunneling diode (RTD) using low band offset dielectric material as double barrier layers and having a vertical layer configuration comprising:

a substrate having a substantially planar horizontal surface;

a horizontally disposed configuration of vertical layers formed on said substrate, said layers being perpendicular to said horizontal surface, said configuration further comprising:

a quantum well layer formed of a semiconductor material, said layer being vertical, having parallel planar vertical sides and being formed to a first thickness;

a tunneling barrier layer formed on each side of said quantum well layer, each said barrier layer being formed, to a second thickness, of a dielectric material characterized by a low band offset relative to the conduction band edge of said semiconductor material; and

an adjacent conducting contact layer being formed on each said tunneling barrier layer.

2. The RTD of claim 1 wherein said quantum well semiconductor material is monocrystalline Si, Ge or SiGe.

3. The RTD of claim 1 wherein said quantum well layer is oriented so that its vertical sides are any preferred crystallographic plane.

4. The RTD of claim 3 wherein said low band offset dielectric material is the high-k dielectric material Si_3N_4, HfO_2, ZrO_2, Y_2O_3, Pr_2O_3, TiO_2, Al_2O_3, or Ta_2O_5, or their alloys or laminates.

5. The RTD of claim 4 wherein said dielectric material is formed to a second thickness of between approximately 0.5 nm. and 5.0 nm.

6. The RTD of claim 5 wherein the quantum well layer is monocrystalline Si and the crystallographic planes are the 100, 110 or 111 crystallographic planes.

7. The RTD of claim 6 wherein said Si quantum well layer is formed to a first thickness between approximately 2 nm. and 25 nm. and wherein said layer is characterized by at least one electron bound state and associated bound state energy.

8. The RTD of claim 7 wherein the silicon quantum well layer is doped with either n-type or p-type doping to a dopant concentration between approximately10^{-16} and 10^{-19} cm^{-3}.

9. The RTD of claim 1 wherein each said conducting layer is a layer of n+ doped polysilicon or a layer of metal.

10. The RTD of claim 1 wherein said substrate is a SOI, GOI or SiGe-on oxide substrate and wherein an isolating layer is interposed between said substrate and said horizontally disposed configuration.

11. A resonant tunneling diode (RTD) using low band offset dielectric material as double barrier layers comprising:

a substrate;

a patterned configuration of planar horizontal layers formed on said substrate and extending partially within said substrate, said configuration having substantially planar vertical sides and the configuration further comprising:

a quantum well layer formed of a semiconductor material, said layer being characterized by upper and lower planar horizontal surfaces and a first thickness;

an upper tunneling barrier layer formed on said upper surface of said quantum well layer and a lower tunneling barrier layer formed on said lower surface of said quantum well layer, each said barrier layer having a substantially equal second thickness and each barrier layer being formed of a dielectric material characterized by a low band offset relative to said quantum well layer;

an upper conducting layer formed on said upper tunneling barrier layer and a lower conducting layer formed beneath said lower tunneling barrier layer and extending substantially into an insulating layer within said substrate; and

said insulating layer being laterally disposed to said lower conducting layer and contacting vertical sides of said conducting layer.

12. The RTD of claim 11 wherein said quantum well semiconductor material is monocrystalline Si, Ge or SiGe.

13 . The RTD of claim 12 wherein said quantum well layer is monocrystalline silicon and it is formed to a first thickness between approximately 2 nm. and 25 nm. and wherein said layer is characterized by at least one electron bound state and associated bound state energy.

14. The RTD of claim 13 wherein the silicon quantum well layer is doped with either n-type or p-type doping to a dopant concentration between approximately10^{-16} and 10^{-19} cm^{-3}.

15. The RTD of claim 12 wherein said low band offset dielectric material is the high-k dielectric material Si_3N_4, HfO_2, ZrO_2, Y_2O_3, Pr_2O_3, TiO_2, Al_2O_3, or Ta_2O_5, or their alloys or laminates.

16. The RTD of claim 15 wherein said dielectric material is formed to a second thickness of between approximately 0.5 nm. and 5.0 nm.

17. The RTD of claim 11 wherein each said conducting layer is a layer of n+ doped polysilicon or a layer of metal.

18. A resonant tunneling diode (RTD) using low band offset dielectric material as double barrier layers comprising:

a substrate;

a patterned configuration of planar horizontal layers formed within an opening in said substrate, said configuration further comprising:

a quantum well layer formed of semiconductor material, said layer being characterized by upper and lower planar horizontal surfaces and a first thickness;

an upper tunneling barrier layer formed on said upper surface and a lower tunneling barrier layer formed on said lower surface of said quantum well layer, each said barrier layer having a substantially equal second thickness and each barrier layer being formed of a dielectric material characterized by a low band offset relative to said quantum well layer;

an upper conducting layer formed on said upper tunneling barrier layer and a lower conducting layer formed on said lower tunneling barrier layer; and

an isolating dielectric layer formed between said lower conducting layer and said substrate; and, wherein said upper conducting layer, said upper barrier layer, said silicon well layer and said lower barrier layer have been patterned to form co-planar vertical sides and a common horizontal cross-section which is substantially square.

19. The RTD of claim 18 wherein said quantum well semiconductor material is monocrystalline Si, Ge or SiGe.

20. The RTD of claim 18 wherein said quantum well layer is monocrystalline silicon and it is formed to a first thickness between approximately 2 nm. and 25 nm. and wherein said layer is characterized by at least one electron bound state and associated bound state energy.

21. The RTD of claim 20 wherein the silicon quantum well layer is doped with either n-type or p-type doping to a dopant concentration between approximately 10^{-16} and 10^{-19} cm^{-3}.

22. The RTD of claim 19 wherein said low band offset dielectric material is the high-k dielectric material Si_3N_4, HfO_2, ZrO_2, Y_2O_3, Pr_2O_3, TiO_2, Al_2O_3, or Ta_2O_5, or their alloys or laminates.

23. The RTD of claim 22 wherein said dielectric material is formed to a second thickness of between approximately 0.5 nm. and 5.0 nm.

24. The RTD of claim 18 wherein each said conducting layer is a layer of n+ doped polysilicon or a layer of metal.

25. A method of forming a resonant tunneling diode (RTD) having tunnel barrier layers formed of low band offset dielectric material and a vertical layer configuration comprising:

providing a substrate having a substantially planar horizontal surface;

forming a horizontally disposed configuration of vertical layers on said substrate, said layers being perpendicular to said horizontal surface, the formation of said configuration further comprising:

forming, by photolithographic patterning and etching, a quantum well layer of a monocrystalline semiconductor material, said layer being vertical, having parallel planar vertical sides and being formed to a first thickness;

smoothing the vertical sides of said quantum well layer;

forming, by a process of CVD, ALD or sputtering, a tunneling barrier layer on each side of said quantum well layer, each said barrier layer being formed, to a second thickness, of a dielectric material characterized by a low band offset relative to the conduction band edge of said quantum well layer;

forming a conducting contact layer on each said tunneling barrier layer; and

smoothing the sides of each said contact layer.

26. The method of claim 25 wherein said substrate is a SOI substrate, a GOI substrate or a SiGe-on-insulator substrate.

27. The method of claim 25 wherein said semiconductor material is monocrystalline Si, Ge or SiGe.

28. The method of claim 27 wherein said low band offset dielectric material is the high-k material Si_3N_4, HfO_2, ZrO_2, Y_2O_3, Pr_2O_3, TiO_2, Al_2O_3, or Ta_2O_5, their alloys or laminates.

29. The method of claim 25 wherein said quantum well layer is oriented so that its vertical sides are in any of its preferred crystallographic planes.

30. The method of claim 29 wherein the layer is Si and its crystallographic planes are the 100, 110 or the 111 crystallographic planes.

31. The method of claim 30 wherein said silicon quantum well layer is formed to a first thickness between approximately 2 nm. and 25 nm. and wherein said layer is characterized by at least one electron bound state and associated bound state energy.

32. The method of claim 31 wherein the silicon quantum well layer is doped with either n-type or p-type doping to a dopant concentration between approximately 10^{-16} and 10^{-19} cm^{-3}.

33. The method of claim 28 wherein said dielectric material is formed to a second thickness of between approximately 0.5 nm. and 3.0 nm.

34. The method of claim 25 wherein said conducting layer is a layer of n+ doped polysilicon or a layer of metal.

35. A method of forming a low band offset double barrier resonant tunneling diode (RTD) having low band offset dielectric material for the barrier layers comprising:

providing a substrate including an upper monocrystalline semiconductor layer, a lower semiconductor layer and a buried oxide (BOX) layer formed between said upper and lower semiconductor layers, wherein said upper semiconductor layer has an upper surface and a lower surface and wherein said buried oxide layer is formed between the lower surface of said upper and said lower semiconductor layers;

etching a trench through said lower semiconductor layer and said BOX layer to expose a portion of said lower surface of said upper semiconductor layer;

forming a lower tunneling barrier layer on said exposed portion of said lower surface of said upper semiconductor layer, said barrier layer being formed of a dielectric material characterized by a low band offset relative to said upper semiconductor layer;

forming a lower conducting layer on said lower barrier layer;

reducing the thickness of said upper semiconductor layer by etching away a

portion of said upper surface of said upper semiconductor layer that is vertically above said lower exposed semiconductor surface, said reduction in thickness producing a quantum well;

forming an upper tunneling barrier layer on said etched upper semiconductor surface said layer being formed of a dielectric material characterized by a low band offset relative to said silicon layer; and

forming an upper conducting layer on said upper tunneling barrier layer.

36. The method of claim 35 wherein said substrate is a SOI substrate, a GOI substrate or a SiGe-on-insulator substrate.

37. The method of claim 35 wherein said semiconductor material is monocrystalline Si, Ge or SiGe.

38. The method of claim 37 wherein said low band offset dielectric material is the high-k material Si_3N_4, HfO_2, ZrO_2, Y_2O_3, Pr_2O_3, TiO_2, Al_2O_3, or Ta_2O_5, their alloys or laminates.

39. The method of claim 30 wherein said quantum well layer is a layer of silicon formed to a first thickness between approximately 2 nm. and 25 nm. and wherein said layer is characterized by at least one electron bound state and associated bound state energy.

40. The method of claim 39 wherein the silicon quantum well layer is doped with either n-type or p-type doping to a dopant concentration between approximately10^{-16} and 10^{-19} cm^{-3}.

41. The method of claim 38 wherein said dielectric material is formed to a second thickness of between approximately 0.5 nm. and 3.0 nm.

42. The method of claim 35 wherein said conducting layer is a layer of n+ doped polysilicon or a layer of metal.

43. A method of forming a resonant tunneling diode (RTD) having low band offset dielectric material for the barrier layers comprising:

providing a substrate including an upper semiconductor layer, a lower semiconductor layer and a buried oxide (BOX) layer formed between said upper and lower semiconductor layers, wherein said upper semiconductor layer has an upper surface and a lower surface and wherein said buried oxide layer is formed between the lower surface of said upper semiconductor layer and said lower semiconductor layer;

forming a patterned configuration of planar horizontal layers on the lower semiconductor layer of said substrate, said formation further comprising:

forming a patterned layer of the upper semiconductor layer, by vertically etching a trench surrounding a substantially square region of said upper layer, the trench passing completely through said BOX layer and terminating at said lower

semiconductor layer, and then removing all portions of said BOX layer directly beneath said patterned upper layer by laterally etching said BOX layer;

forming a lower tunneling barrier layer on the lower surface of said patterned layer by a lateral deposition, said barrier layer being formed of a dielectric material characterized by a low band offset relative to said upper semiconductor layer; said deposition also forming a dielectric isolation layer on said lower semiconductor layer;

forming a lower conducting layer on said lower tunneling barrier layer by lateral deposition, said conducting layer being, thereby, between said tunneling barrier layer and said isolation layer;

thinning said patterned upper semiconductor layer to form a quantum well layer;

forming an upper tunneling barrier layer on the upper surface of said quantum well layer by deposition, said upper tunneling barrier layer being formed of a dielectric material characterized by a low band offset relative to said silicon layer;

forming an upper conducting layer on said upper tunneling barrier layer by deposition;

patterning said upper conducting layer to produce a layered configuration of substantially square horizontal cross-section and substantially planar vertical sides, said layered configuration including the lower barrier layer, the upper silicon layer, the upper barrier layer and the upper conducting layer.

44. The method of claim 43 wherein said tunneling barrier layers and said conducting layers are deposited by CVD.

45. The method of claim 43 wherein said substrate is a SOI substrate, a GOI substrate or a SiGe-on-insulator substrate.

46. The method of claim 43 wherein said semiconductor material is monocrystalline Si, Ge or SiGe.

47. The method of claim 43 wherein said low band offset dielectric material is the high-k material Si_3N_4, HfO_2, ZrO_2, Y_2O_3, Pr_2O_3, TiO_2, Al_2O_3, or Ta_2O_5, their alloys or laminates.

48. The method of claim 47 wherein said quantum well layer is a layer of silicon formed to a first thickness between approximately 2 nm. and 25 nm. and wherein said layer is characterized by at least one electron bound state and associated bound state energy.

49. The method of claim 48 wherein the silicon quantum well layer is doped with either n-type or p-type doping to a dopant concentration between approximately 10^{-16} and 10^{-19} cm^{-3}.

50. The method of claim 47 wherein said dielectric material is formed to a second thickness of between approximately 0.5 nm. and 3.0 nm.

51. The method of claim 43 wherein said conducting layer is a layer of n+ doped polysilicon or a layer of metal.